UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,289	12/28/2001	Young-Hun Ha	8733.560.00	2930

30827 7590 03/27/2003

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER
DI GRAZIO, JEANNE A

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 03/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,289	HA ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Priority to Korean Patent Application No. 2000-85421 (Dec. 29, 2000) is claimed.

Claim Objections

Claims 19 and 20 are objected to because of the following informalities: Claims 19 and 20 depend upon claim 23 when they should depend on claim 18. There are only 20 claims pending. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae (US 2002/0030769 A1) in view of Nishiguchi et al. (US '553).

Per claim 1: Bae has a lower substrate with a seal pattern forming region [0017]. Bae has an upper substrate [0017] and a liquid crystal layer between the upper and lower substrate [0017]. Bae also has a passivation layer removed in the sealant region [0064]. Bae does not appear to specify that the seal pattern is formed between a display area and a non-display area; however, Nishiguchi does have sealing material in a non-display section side in a boundary region between the display section and the non-display section (Col. 4, Lines 10-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Nishiguchi for reduced unevenness of tone and improved display quality

(See Nishiguchi at Col. 4, Lines 31-38) and also for enhanced adhesion and high yield (See Bae at 0003).

Per claim 2: Bae does not appear to specify a first substrate with a display and non-display area; however, Nishiguchi has each substrate that has a display and non-display section (Col. 3, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Nishiguchi so that surfaces of the substrates on which electrodes are respectively formed face each other (Nishiguchi, Col. 3, Lines 61-65).

Per claim 6: Bae does have spacers sprayed over a substrate [0018 / conventional art]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include spacers for maintaining substrate gap.

2. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bae (US 2002/0030769 A1) and Nishiguchi et al. (US '553) in further view of Kim et al. (US '050 B1).

Per claim 3: Bae does not appear to have a gate electrode on a substrate, a gate insulating layer on the gate electrode, a TFT on the gate insulating layer, a pixel electrode that is connected to the TFT on the gate insulating film and a passivation layer on the TFT; however, Kim recites this complete structure (SEE FIGURE 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Kim for good display characteristic, high aperture ratio, and high yield (Col. 2, Lines 28-30 of Kim) and for manufacturing ease.

3. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae (US 2002/0030769 A1) and Nishiguchi et al. (US '553) in further view of Kim et al. (US '794 B1).

Per claim 4: Bae does not appear to have a second substrate with a color filter and common electrode there on; however, Kim (794) has a color filter on a second substrate, and a common electrode on the color filter layer (Col. 2, Lines 22-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Kim (794) in part for a wide viewing angle as noted in Kim.

Per claim 7: Bae has the step of forming a substrate with a passivation layer removed in the seal region as noted. Bae does not appear to have the step of forming an upper substrate including a second substrate, color filter, and common electrode; however, Kim (794) as noted has this step. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Kim (794) in part for a wide viewing angle as noted in Kim. Bae has the step of forming spacers between upper and lower substrates as noted for uniformity of cell spacing as noted. Bae has the step of assembling the substrates and injecting liquid crystal into an interior of the seal pattern [0020]. Bae also has the step of forming a seal pattern wherein the seal pattern contacts a gate insulating layer [0076]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the seal pattern contact a gate insulating layer for improved adhesion as noted in Bae.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bae (US 2002/0030769 A1) and Nishiguchi et al. (US '553) in further view of Kwak et al. (US '940 B2).

Per claim 5: Bae has a passivation layer removed in the area of the seal region. Bae does not appear to specify that the passivation layer is removed for simultaneous patterning of the active and passivation layer; however, Kwak has simultaneous patterning of the passivation and active layer (Col. 2, Lines 52-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Kwak for removal of the passivation layer for simultaneous patterning of the active and passivation layers to reduce the number of mask steps.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bae (US 2002/0030769 A1) and Kim et al. (US '794 B1) in further view of Kim et al. (US '050 B1).

Per claim 8: Bae does not appear to have the steps of forming: a gate electrode on a substrate, a gate insulating layer on the gate electrode, a TFT on the gate insulating layer, a pixel electrode that is connected to the TFT on the gate insulating film and a passivation layer on the TFT; however, Kim recites this complete structure (SEE FIGURE 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bae in view of Kim for good display characteristic, high aperture ratio, and high yield (Col. 2, Lines 28-30 of Kim) and for manufacturing ease.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US '050 B1) in view of Nishiguchi et al. (US '553), Bae (US 2002/0030769 A1) and Kim et al. (US '794 B1).

Per claim 9: Kim (050) has: a lower substrate and first substrate, a gate electrode on the first substrate, a gate insulating layer on the first substrate and on the gate electrode, a TFT on

the gate insulating layer, a pixel electrode on the gate insulating layer, the pixel electrode being connected to the TFT, and a passivation layer on the TFT (Figure 5) as noted. Kim does not appear to have a lower substrate divided into a display and non-display area with a seal pattern forming region between the display and non-display area of a lower substrate and a seal pattern formed in a boundary region between the display and non-display area of a lower substrate; however, as noted, Nishiguchi meets these limitations (Col. 3, Lines 60-65 and Col. 4, Lines 10-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim in view of Nishiguchi so that surfaces of the substrates on which electrodes are respectively formed face each other (Nishiguchi, Col. 3, Lines 61-65).

Kim (050) does not appear to have a passivation layer removed in the seal region; however, as noted in Bae, Bae has a passivation layer removed in a seal region [0064]. Bae also has liquid crystal between substrates [0020, for example]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim (050) in view of Bae for enhanced adhesion and high yield (See Bae at 0003).

Kim (050) does not appear to have a second substrate with a color filter and common electrode; however, Kim (794) has a color filter on a second substrate, and a common electrode on the color filter layer (Col. 2, Lines 22-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim (050) in view of Kim (794) in part for a wide viewing angle as noted in Kim.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi et al. (US '553) in view of Kazlas et al. (US '606).

Per claim 10: Nishiguchi has substrates facing each other wherein each substrate has display and non-display regions (Col. 3, Lines 60-65). Nishiguchi has a seal pattern formed between the substrates along a boundary region between display and non-display sections (Col. 4, Lines 10-15). Nishiguchi has an injection hole (Example 2, Col. 8, Lines 22-23) for injecting liquid crystal. The injection hole is then sealed (Id.). Nishiguchi does not appear to have the seal pattern serving as a cell gap for injecting liquid crystal and to bond the substrates; however, Kazlas has a photo-definable polymeric resin as both an edge seal and a spacer [For example, ABS]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Kazlas for a thin, uniform device in which the number of mask steps is reduced because the resin serves dual functions, that of seal and spacer concurrently.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi et al. (US '553) and Kazlas et al. (US '606) in further view of Tsubota et al. (US '787).

Per claim 11: Nishiguchi does not appear to have a seal pattern formed by a screen printing process using a thermosetting resin that includes a glass fiber; however, Tsubota has a seal pattern formed by screen printing (Col. 2, Lines 24-27) and that includes glass fiber (Col. 17, Lines 63-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Tsubota for ease in curing the seal and the resin including glass fibers may be used as spacers for uniform gap control.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US '050 B1) in view of Nishiguchi et al. (US '553).

Per claim 12: Kim (050) has: a lower substrate and upper substrate apart and facing each other, a gate electrode on a substrate, a gate insulating layer completely over a substrate and on the gate electrode, a TFT and gate electrode on the gate insulating layer, a pixel electrode on the gate insulating layer, the pixel electrode being connected to the TFT, and a passivation layer on the TFT (Figure 5) as noted. Kim does not appear to have a seal pattern formed between substrates in a boundary region between the display and non-display area of a lower substrate; however, as noted, Nishiguchi meets these limitations (Col. 3, Lines 60-65 and Col. 4, Lines 10-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim in view of Nishiguchi so that surfaces of the substrates on which electrodes are respectively formed face each other (Nishiguchi, Col. 3, Lines 61-65). Nishiguchi furthermore has spacers for uniform cell gap as previously noted.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US '579 B1) in view of Aoki et al. (US '838), Kohei et al. (JP 11-326949), Ikeda (US '729 B1), and Nishiguchi et al. (US '553) and Bae (US 2002/0030769 A1).

Per claim 13: Lim et al. has a plurality of gate lines including a gate electrode and capacitor electrode on an array substrate (Col. 3, Lines 35, 61 and Col. 4, Lines 16-17). Lim also has a plurality of data lines including a drain electrode (Col. 3, Line 36 and Col. 4, Lines 5-6). The gate and data lines cross each other (Col. 3, Lines 36-37). Lim also has gate and data pads formed at one end of the gate and data lines (Col. 2, Lines 59-61). Lim also has source and drain electrodes spaced apart from each other (Figure 5c). Typically, pixel electrodes are connected to source electrodes (For example, See Byun et al. US '199)(stating that source electrodes are in electrical communication with pixel electrodes at Col. 1, Lines 63-67). Lim furthermore has a

pixel electrode (135) partially overlapping with a first capacitor electrode (123)(referring to Figure 6a). Lim has a semiconductor layer (39) (Prior Art, Figures 2b and 2c) forming a semiconductor channel region (53) below source (45) and drain electrodes (47). Lim does not appear to have the semiconductor layer under source and drain electrodes including the TFT including the gate electrode; however, Aoki has a semiconductor layer (21) formed underneath TFTs (16) and including the gate electrode (23) (referring to Figure 12 I). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Aoki so that contamination of semiconductor layers can be prevented, sufficient insulation can be had between the source / drain and gate electrodes, high contrast, and to prevent breaking of elements in the structure (Aoki at Col. 3, Lines 40-62 et al.). Lim does not appear to have an auxiliary capacitance electrode electrically connected to a pixel electrode; however, Kohei has a pixel electrode and auxiliary capacity electrode electrically connected to each other (PAJ). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Kohei to reduce the number of process steps as noted in Kohei (PAJ). Lim does not appear to have the auxiliary capacitance electrode formed between the capacitance and pixel electrode; however, Ikeda has an auxiliary capacitance electrode between the capacitance electrode and the pixel electrode (Col. 1, Lines 50-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Ikeda for a common storage type capacitor as noted in Ikeda (Id.). Lim does not appear to have a seal pattern formed between a data pad and adjacent portion of a data line to assemble substrates with a uniform cell gap; however, Yamamoto et al. (US '460) has a sealant forming around a periphery of a drive circuit (Figure 6). It would have been obvious to

one of ordinary skill in the art at the time the invention was made to modify Lim in view of Yamamoto for ease in repair of disconnection as noted in Yamamoto. Lim does not appear to have a seal pattern dividing the array substrate into display and non-display regions; however, as noted, Nishiguchi has this limitation. Nishiguchi has each substrate that has a display and non-display section (Col. 3, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Nishiguchi so that surfaces of the substrates on which electrodes are respectively formed face each other (Nishiguchi, Col. 3, Lines 61-65). Lim does not appear to have a passivation layer removed in an area where electric lines are not formed; however, Bae has a passivation layer removed in the sealant region [0064] where the sealant region is on the boundary between display and non-display regions as noted. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Bae for improved adhesion and uniform substrate gap.

11. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rho et al. (US '146 B1) in view of Hoffmann et al. (US '471) and Kim et al. (US '516 B1).

Per claim 14: Rho has substrates and a spacer disposed between the substrates, a storage capacitor including a capacitance electrode formed on a transparent substrate (Col. 2, Lines 38-42), a gate insulating layer formed on the transparent substrate and on the capacitance electrode (Figure 4), and a semiconductor layer formed on the gate insulating layer / transparent substrate (Figure 4). Rho does not appear to specify an auxiliary capacitance electrode formed on the semiconductor layer; however, Hoffmann has a storage capacitor and storage capacitor electrode arranged above a doped semiconductor layer [ABS.]. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify Rho in view of Hoffmann for reduced size (area) of the array device as noted in Hoffmann. Rho has a pixel electrode formed on a passivation layer (Figure 4). Rho does not appear to have a pixel electrode contacting a lateral side of an auxiliary capacitance electrode; however, Kim has such an arrangement (Figures 6 and 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rho in view of Kim for increased scanning time and for improved image quality as noted in Kim.

Per claims 15-16: Rho has a gate electrode on a transparent substrate, a gate insulating layer on the transparent substrate and on the gate electrode, and a source and drain electrode spaced apart from each other and formed on a semiconductor layer. Rho also has a semiconductor layer including an active layer and an ohmic contact layer where the semicondcutor layer is formed on the gate insulating layer (Figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include these limitations in part to reduce coupling capacitance, and increase aperture ration as noted in Rho at Col. 2, Lines 1-21.

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rho et al. (US '146 B1), Hoffmann et al. (US '471) and Kim et al. (US '516 B1) in further view of Song et al. (US '392 B2).

Per claim 17: Rho does not appear to have only the gate insulating layer formed on the transparent substrate in the boundary region between the display and non-display areas to maintain gap distance; however, Song has a gate insulating layer in the display area but the gate insulating layer in the peripheral area is completely removed (Col. 12, Lines 9-13). It would have

been obvious to one of ordinary skill in the art at the time the invention was made to modify Rho in view of Song for improved bonding of the substrate and for improved adhesion.

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi et al. (US '553) in view of Kim et al. (US '050 B1), Bae (US 2002/0030769 A1), Kim et al. (US '794 B1), and Kwak et al. (US 2001/0013918 A1) in view of Saito et al. (US '308 B1).

Per claim 18: Nishiguchi has substrates divided into display and non-display areas as noted previously. Nishiguchi does not appear to have a gate electrode on a substrate, a gate insulating layer on the gate electrode, a TFT on the gate insulating layer, a pixel electrode that is connected to the TFT on the gate insulating film and a passivation layer formed on the TFT; however, Kim (050) has these elements (Figure 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Kim for good display characteristic, high aperture ratio, and high yield (Col. 2, Lines 28-30 of Kim) and for manufacturing ease. Nishiguchi does not appear to have a passivation layer formed on a seal region that is etched away during photolithography and the seal pattern formed directly on the gate insulating layer; however, Bae has a passivation layer removed in the sealant region [0064]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Bae for improved adhesion. Nishiguchi does not appear to have the seal pattern formed directly on the gate insulating layer; however, Kwak has a sealant on a gate insulating layer (See claim 28 of Kwak). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Kwak for reduced mask steps. Nishiguchi does not appear to have a second substrate with a color

filter and common electrode there on; however, Kim (794) has a color filter on a second substrate, and a common electrode on the color filter layer (Col. 2, Lines 22-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Kim (794) in part for a wide viewing angle as noted in Kim. Nishiguchi does not appear to have the steps of providing spacers in the display area, the forming a seal pattern with an injection hole (on one or both substrates), injecting LC and sealing an injection hole of the seal pattern; however, Saito has these general steps (Col. 8, Lines 40-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Saito for manufacturing ease and reduced process steps and also to prevent contamination of the liquid crystal.

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi et al. (US '553), Kim et al. (US '050 B1), Bae (US 2002/0030769 A1), Kim et al. (US '794 B1), Kwak et al. (US 2001/0013918 A1), and of Saito et al. (US '308 B1) in further view of Stein et al. (US '860 B1).

Per claim 19: Nishiguchi does not appear to have an alignment coating process and a rubbing process preced the spacer dispensing process and seal pattern forming process; however, Stein has these limitation steps (Col. 12, Lines 23-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Stein for manufacturing simplicity and efficiency.

15. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi et al. (US '553), Kim et al. (US '050 B1), Bae (US 2002/0030769

A1), Kim et al. (US '794 B1), Kwak et al. (US 2001/0013918 A1), and Saito et al. (US '308 B1) in further view of Kwak et al. (US '940 B2).

Per claim 20: Nishiguchi does not appear to specify that the passivation layer is removed for simultaneous patterning of the active and passivation layer; however, Kwak has simultaneous patterning of the passivation and active layer (Col. 2, Lines 52-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nishiguchi in view of Kwak for removal of the passivation layer for simultaneous patterning of the active and passivation layers to reduce the number of mask steps.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (703)305-7009. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (703) 305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-8741 for regular communications and (703)746-8741 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jeanne Andrea Di Grazio

JDG
March 24, 2003

Robert Kim, SPE

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800